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Mixer DesignGuide Reference

The Mixer DesignGuide is integrated into the Agilent EEsof Advanced Design System. It contains many analysis schematics and data displays that are useful for the design and analysis of RFIC mixers or the application of discrete mixers in RF systems. This DesignGuide is not a complete solution for mixer and RF system designers, but will provide you with some useful tools. It is intended to save you time in setting up schematics and displays.

Note

It is essential that you use verified nonlinear transistor models for the specific process that you will be using to fabricate your mixer. S-parameters are linear small-signal parameters and will not be useful for this purpose. Mixer simulations are very sensitive to the device model because their primary function requires nonlinear operation, either by device nonlinearity or by switching (a large-signal process). Making accurate predictions of gain compression, intermodulation distortion, and calculating intercepts requires models with accurate nonlinearity up to the order of distortion you are simulating.

This DesignGuide provides some generic models for 0.25mm and 0.35mm NMOS and PMOS FETs and a generic BJT. These models are used in the schematic templates to provide examples of how to use the analysis tools, but will not be valid for your specific design.

Schematic and display templates are copied into your workspace when a simulation type is selected. Data from the default simulation is also provided. You should replace the mixer (or divider/doubler) subnetwork with your own and modify the simulation parameters as needed (see the following discussion). The data display may consist of two or more pages. Typically, equations are placed on a separate page. Occasionally, the data displayed may be broken up into separate display pages. Select these using the Page menu.

Mixer Selection

The Mixer Design Guide is organized according to the typical choices and steps for the design and analysis of mixers. First, you will need to decide what type of mixer you are evaluating and whether you will be using it to convert down or up. There are a very large variety of circuit techniques that can provide the mixing operation. If the mixer inputs are at ω_1 and ω_2 , the mixer must provide outputs at $\omega_1 + \omega_2$ and $\omega_1 - \omega_2$. The mixer will make use of either device characteristics with second-order nonlinearity or modulation of the signal path with a switch driven by the local oscillator to produce these terms.

The best mixers generally are the switching type since they will often lead to fewer spurious outputs (spurs) and can be made to have higher gain compression thresholds. The superior performance is obtained by making sure that the signal path is as linear as possible. This technique is preferred at all frequencies low enough to permit an accurately controlled switching operation. Nonlinear mixers are still used occasionally for millimeter wave applications or noncritical lower frequency uses.

Balancing is also often employed to reduce the number of spurs. Refer to *S. Long, Fundamentals of Mixer Design, Agilent EEsof Design Seminar, 1999* for a description of mixer operation and the important figures of merit associated with mixer performance. As shown below, the DesignGuide also provides a sample library of representative mixer types that you can experiment with or modify for your own use.

[Mixer Circuit Library](#)

Mixer Type	I/O	Balance	RF frequency	Design File Name
	Single Ended	Double	wideband	DIODEDB1_mix
	Single Ended	Double	wideband	FETring_mix
	Differential	Double	wideband	FETring_Diff_mix
	Single ended	Unbalanced	900 MHz	FET1_mix
	Single Ended	Double	900 MHz	Gilbert_SE_mix
	Single Ended	Double	900 MHz	Gilbert_SEbias_mix
	Differential	Double	wideband	Gilbert_Dbias_mix
MOS Gilbert cell w. bias.	Differential	Double	1800 MHz	Diff_MixerUnderTest_Tuned
MOS Gilbert cell w. bias.	Differential	Double	1800 MHz	Diff_MixerUnderTest_Tuned_D2SE
	Single Ended	Unbalanced	wideband	SE_Mixer
	Single Ended	Double	wideband	GilCellMix
BJT Gilbert Cell	Differential	Double	wideband	BJT_Diff_MixerUnderTest

You will be able to use the Mixer DesignGuide most efficiently if you understand what it does when you make menu selections. When you make a menu selection, for example, *Mixer DesignGuide > Differential Mixer Characterization > IF Spect., Isolation, Conv. Gain, Port Impedances*, a schematic (in this case, *Mix_Diff_Spect_Iso*) with a sample mixer, *Diff_MixerUnderTest*, and a corresponding data display are copied into your workspace.

All of the mixer characterization menu picks copy similar schematics with either the differential sample mixer, *Diff_MixerUnderTest*, or the single-ended sample mixer, *SE_MixerUnderTest*. However, before the Mixer DesignGuide copies schematics, subcircuits, or data displays into your workspace, it checks to see if files with the same names already exist in your workspace. Any files that already exist will not be overwritten. You should push into the sample mixer subcircuit, and modify the schematic or paste your mixer schematic into the subcircuit. You will only have to do this once, as all subsequent mixer characterization schematics inserted via menu picks will use the same subcircuit, named *Diff_MixerUnderTest* or *SE_MixerUnderTest*.

Before using the DesignGuide:

1. Choose a mixer type (Active or Passive).
An active mixer is one that can provide power (conversion) gain from RF to IF. The widely used double-balanced XOR (Gilbert or Jones) style of mixer is an example of an active mixer that is provided in the DesignGuide mixer library. A passive mixer is one that can only provide conversion loss. For example, the FET double-balanced ring or diode double-balanced ring mixers are popular examples also included in the library. It is often easier to obtain large gain compression threshold and intercept point with passive mixers.
2. Choose an I/O configuration (Single-ended or Differential).
This is an important design decision. Differential is generally preferred for RFIC applications, as it lends itself to double balancing without the need for passive baluns or transformers. There is also an advantage in rejection of noise coupled through the substrate due to common-mode rejection. However, if the differential interface on-chip is provided by active *baluns*, the gain compression and intermodulation performance are often limited by the single-ended to differential conversion stage at the input to the mixer. The input *balun* is often implemented as the output of a low noise amplifier.
3. Choose an application (Down conversion or Up conversion).
This choice is clearly dictated by your requirements for RF, LO and IF frequencies. Note that in all mixer characterization schematics, *RFfreq* is the variable defining the input signal frequency and *IFFreq* is the variable defining the output frequency. If *RFfreq* is higher than *IFFreq*, the simulation is set up for down conversion. If you want to simulate up conversion, just define *RFfreq* and *IFFreq* such that *IFFreq > RFfreq*.

DC Analysis

A good place to begin designing either active or passive mixers is with the DC characteristics of the transistor. The purpose for the DC analysis is to establish appropriate bias conditions for the device areas or widths needed in your mixer. In the case of active mixers, bias voltages and currents should be selected for the signal path elements that provide for the best tradeoff between linearity, noise figure, and to minimize compression and distortion at large signal levels.

The DC characterization is useful to the extent that it clarifies the range of operating conditions possible without driving the device into the ohmic or cutoff regions. The designer will need to perform additional analyses to determine the optimum conditions for the above performance measures, since these limits can't be predicted solely by DC evaluations. These other parameterized simulations will be described in a later section. In the case of passive mixers, estimates can be made of R_{on} for selected channel widths and V_{GS} drive levels that will guide the initial design.

In this DesignGuide, under the command sequence DesignGuide > Mixer DesignGuide > Device Characterization, we have included schematics and displays for simulation of DC I-V characteristics of NMOS, PMOS and BJT devices as shown below. Some generic BSIM3 device models for 0.25 μ m and 0.35 μ m MOSFETs have also been provided.

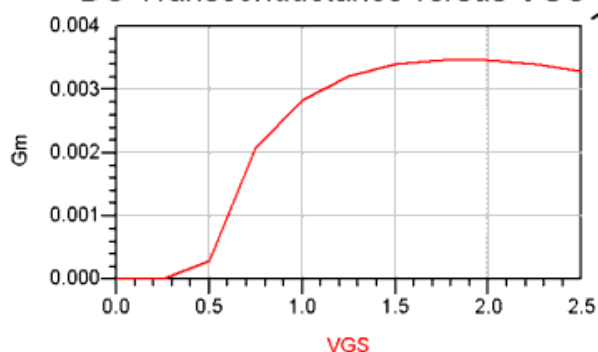
DC Device and Mixer Simulation files

Analysis	Schematic ()	Display
Evaluate device ID - VDS	NMOS_curve_tracer	NMOS_curve_tracer
Evaluate mixer DC biasing	Mix_SE_DC	N/A
0.25 μ m MOSFET BSIM3 model	mos25	N/A
0.35 μ m MOSFET BSIM3 model	mos35	N/A

These curve-tracer like simulations can be used to help select appropriate bias voltages and currents or to select device widths. For example, in [DC Transconductance versus \$V_{GS}\$ for a 0.25 \$\mu\$ m x 10 \$\mu\$ m NMOS device](#), we can see that a V_{GS} of 1 V or higher is desired in

order to obtain close to maximum G_m . Refer to *S. Long, RFIC MOS Gilbert Cell Mixer Design, Agilent EESOF Design Seminar, 1999* for a detailed example that discusses the selection of bias currents and device sizes in this commonly-used type of active mixer.

DC Transconductance versus V_{GS}



DC Transconductance versus V_{GS} for a 0.25 μ m x 10 μ m NMOS device.

To use the MOS curve tracer schematic (NMOS_curve_tracer or PMOS_curve_tracer) for your design, replace the default device models with your own verified nonlinear device models. Make sure the gate length and width of the model match the parameters L_G and

W_1 specified in the VarEqn block shown in [Setting bulk-to-substrate voltage, \$V_{sub}\$, channel width, \$W_1\$, and gate length, \$LG\$.](#)

Var Eqn

VAR
VAR1

1. $V_{sub}=0\text{ V}$
 $W_1=1\text{e-}5$
 $LG=2.5\text{e-}7$

Set $V_{sub} = V_{BS}$
Set channel width W_1
Set gate length LG
select model

[Setting bulk-to-substrate voltage, \$V_{sub}\$, channel width, \$W_1\$, and gate length, \$LG\$.](#)

Choose the appropriate range for V_{GS} and V_{DS} as shown in [Sweep range for \$V_{GS}\$ and \$V_{D}\$.](#)

SimInstanceName[6]=

Start=0 Set gate voltage sweep
Stop=-2.5 limits as needed.
Step=-0.25



DC
DC1
SweepVar="VDS"

Start=0 Set drain voltage sweep
Stop=-2.5 limits as needed.
Step=-0.1

Other=OutVar="MOSFET1.Gm" OutVar="W1"

[Sweep range for \$V_{GS}\$ and \$V_{D}\$](#)

Two sample schematic files, Mix_SE_DC and Mix_Diff_DC, have been provided to show how to perform DC simulations of active mixer circuits. You can substitute your own mixer as a subnetwork for the default (Gilbert) mixer used in these examples.

AC and Harmonic Balance Analysis

Once the mixer device widths and biasing conditions have been estimated by the dc analysis procedures, you must perform other analyses in order to evaluate and optimize the ac performance. You can follow a sequence of schematics and displays which will lead you through the process of mixer analysis.

Note

The schematic and display files associated with these simulations are listed in *Schematics and displays for N-dB gain compression through Circuit envelope simulations for digital modulation*. Note that the filename convention Mix_XX_Analysis_Parameter is used throughout this DesignGuide for analysis schematic files. XX can represent either Single-Ended (SE) or differential (Diff) I/O. Analysis is an abbreviation for the simulation type, and the Parameter field is appended when frequency, power, or an arbitrary design parameter is being swept as part of the analysis.

In all mixer characterization schematics, Rf_{freq} is the variable defining the input signal frequency and If_{freq} is the variable defining the output frequency. If Rf_{freq} is higher than If_{freq} , the simulation is set up for down conversion. If you want to simulate up conversion, just define Rf_{freq} and If_{freq} such that $If_{freq} > Rf_{freq}$.

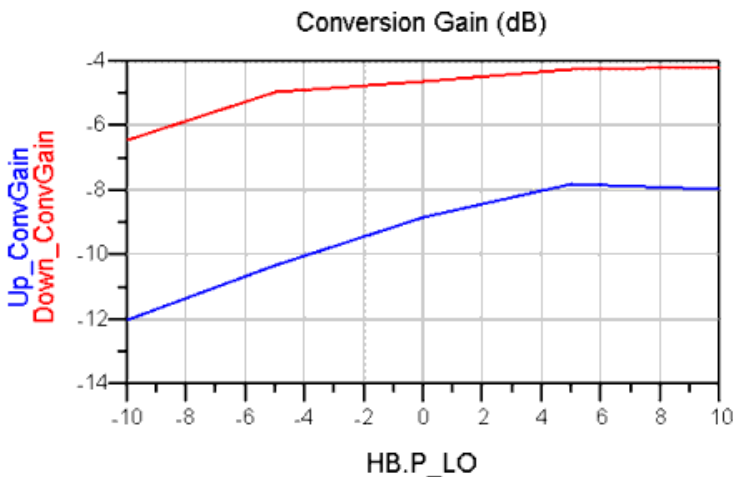
Conversion Gain and Gain Compression

The design sequence for passive or active mixers would begin with the evaluation of conversion gain. The theoretical maximum conversion gain is actually a loss for passive mixers: -10 dB for unbalanced or singly-balanced and -4 dB for double balanced designs. For active mixer designs, gain is possible, but must be considered later as a design variable to be traded off against gain compression and intermodulation performance. Several factors will affect the conversion gain including local oscillator (LO) drive level, impedance matching, and device widths.

Each of these should be evaluated to verify that the mixer is performing with the expected gain level. Parametric sweep templates are provided for this purpose. For example, if the LO drive level is too low, the switching devices may switch to the *on* state but have too much series resistance. This will increase the loss and will also affect the large signal performance.

A good place to begin the design is by evaluating conversion gain with a LO power sweep. The schematic files `Mix_XX_CG_LOswp` and display files `Mix_XX_CG_LOswp.dds` (accessed by the menu selection *Mixer DesignGuide > Differential Mixer Characterization versus LO Power > Isolation, Conv. Gain, Port Impedances* or the corresponding menu selection for single-ended mixers) can be used for this purpose. [Conversion gain as a function of LO power for a differential active mixer from display file `Mix_Diff_CG_LOswp.dds`](#) shows a plot of conversion gain vs. LO power for a representative differential active mixer. You can see that the gain will saturate as the LO drive increases.

A gain compression simulation that includes a LO power sweep should also be performed. Occasionally the gain compression input power level (*PNdB*) will be more sensitive to the LO drive power than the conversion gain, so both should be evaluated. The schematic files `Mix_XX_PNdB_LOswp` (accessed by the menu selection *Mixer DesignGuide > Differential Mixer Characterization versus LO Power > N-dB Gain Compression Point* or the corresponding menu selection for single-ended mixers) will evaluate gain compression and conversion gain (at the compressed level). The LO amplitude should be increased until the 1 dB (or other gain compression level, *N*, of your choice) and the conversion gain no longer change significantly with further increases in LO power.



Conversion gain as a function of LO power for a differential active mixer from display file `Mix_Diff_CG_LOswp.dds`

The following table gives an example of the output of a 1dB gain compression simulation on an active mixer. You can see that the conversion gain is still increasing up to 0 dBm input power but the P1dB input power level has essentially saturated.

Gain Compression Simulation Result

LO Power	LO Voltage	1.0 dB gain compression input power level (dBm)	Conversion
-10	0.188/-20.3	-7.34	-7.70
-5	0.341/-18.0	-7.29	-5.97
0	0.612/-16.1	-7.44	-5.03

Schematics and displays for N-dB gain compression gives mixer design files for gain compression simulations. The menu selections that access these files all end in *N-dB Gain Compression Point*.

Schematics and displays for N-dB gain compression

Analysis	Schematic	Display
Input power for N dB of gain compression	Mix_SE_PNdB	Mix_SE_PNdB
Input power for N dB of gain compression vs. LO power	Mix_SE_PNdB_LOswp	Mix_SE_PNdB_LOswp
Input power for N dB of gain compression vs. swept parameter	Mix_SE_PNdB_PRMswp	Mix_SE_PNdB_PRMswp
Input power for N dB of gain compression vs. RF frequency	Mix_SE_PNdB_FRFswp	Mix_SE_PNdB_FRFswp

Mixer Input and Output Matching

Secondly, the design process depends on whether the mixer input and output must be matched to some off-chip impedance source or load, or if the mixer is interconnected on-chip. When needed, matching networks will provide some passive gain and so should be designed before going further with evaluation and optimization of the large-signal performance or noise figure of the mixer. On-chip interconnections should be modeled with appropriate source and load impedances. These may be complex impedances at a single frequency in some cases or if a wider bandwidth design is required, the source and load could be modeled with equivalent circuits.

The *Mix_XX_Spect_Iso*, *Mix_XX_CG_LOswp*, *Mix_XX_CG_FRFswp*, and *Mix_XX_CG_PRMswp* templates also provide the mixer RF and LO input and IF output port impedances and S-parameters. These files are selected by the first menu selection under each of the *...Mixer Characterization...* menus. This analysis uses the Harmonic Balance simulation method so that these port parameters are measured with the actual large signal LO drive activating the mixer. A small-signal S-parameter simulation could not do this. The parameter sweeps include LO power, RF frequency (with either fixed LO frequency or fixed IF frequency) and a user-defined parameter sweep. Use the *Mix_XX_Spect_Iso.dds*, *Mix_XX_CG_LOswp.dds*, *Mix_XX_CG_FRFswp.dds*, and *Mix_XX_CG_PRMswp.dds* display files that correspond to the schematics above. Schematic and display file are also provided for the design of two element and multi-element matching networks. These are accessed via the *Lumped 2-Element Z-Y Matching Networks* and *Lumped Multi-Element Z-Y Matching Networks* menu selections. These can work with either admittances or impedances and are useful for narrowband designs.

Spectrum and Isolation

Now that matching network(s), if any, have been added, the mixer IF output and RF input spectra can be viewed using *Mix_XX_Spect_Iso* and *Mix_Spect_Iso.dds*. This can be used with the assistance of markers to identify spurious outputs.

Isolation ratios can also be predicted and displayed with these files and with the same simulation and display files described above for port impedance analysis. The isolation ratio indicates how effectively your mixer will attenuate LO at the RF and IF inputs and RF at the IF output.

Note

You should note that very large ratios are sometimes predicted when ideal components are used in balanced mixers. Real components will not be truly identical, and the mismatch in device currents, resistor values, transformer balance, as well as other factors all will degrade the isolation. The sample mixers have been intentionally modified to introduce a realistic amount of unbalance. You will need to do the same for your mixer from your knowledge of the relevant process S-parameter or component variances.

The following table shows IF spectrum, Conversion Gain, Isolation and Port Impedance Simulations.

IF spectrum, Conversion Gain, Isolation and Port Impedance Simulations

Analysis	Schematic	Display
Mixer IF and RF spectra; port-to-port isolation; conversion gain, port impedances.	Mix_SE_Spect_Iso	Mix_SE_Spect_Iso
Conversion gain, isolation and port impedances vs. LO power	Mix_SE_CG_LOswp	Mix_SE_CG_LOswp
Conversion gain, isolation and port impedance vs. swept parameter	Mix_SE_CG_PRMSwp	Mix_SE_CG_PRMSwp
Conversion gain, isolation and port impedance vs. RF frequency	Mix_SE_CG_FRFswp	Mix_SE_CG_FRFswp

Noise Figure or Large Signal?

Once the correct LO power level is determined and matching networks (if needed) are designed, then you should proceed with both a noise figure and a large signal evaluation. Which one you do first depends on which one of these is most critical for your application. The mixer design approaches for low noise and for large signal handling often are in conflict, so tradeoffs must be made to favor whichever is most critical.

Noise Figure

Two sets of schematic files are available for the mixer noise simulations, one for single sideband NF and the other for "All Sideband" NF. Single sideband noise factor is calculated from the following equation

$$F = \frac{v_n^2 / R_L + kT_0(G_1 + G_2 + G_3 + \dots + G_n)}{kT_0 G_1}$$

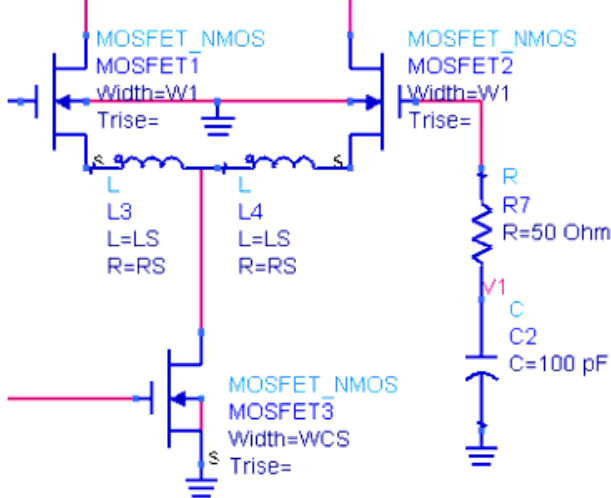
The single sideband noise figure simulation assumes that the signal input to the mixer is from one RF input frequency only (Rffreq). This is normally the case for most mixer applications where an input preselecting filter is applied. In the equation above, the output noise power from the mixer, v_n^2 / R_L , is added to the input noise power kT_0 multiplied by the transducer gains at both mixer input images (G_1 and G_2) plus the gains related to mixing from the higher order LO harmonics (G_3 to G_n). This is in agreement with the IEEE Standard for mixer noise figure [4].

In addition, the noise figure schematics in this DesignGuide also include the noise contribution from the output termination. This can be an important contributor to the total noise when the mixer noise figure is small or for simulation of passive and bilateral mixers such as the diode ring mixer. In the latter case, noise power from the load can be remixed and add significantly to the total noise figure of the mixer [3]. Any noise contribution due to transformer baluns is not included.

Refer to Mix_XX_SSBNF schematic and Mix_XX_SSBNF.dds display files for this simulation at fixed LO power, IF frequency, and design parameters. You may also choose to evaluate the SSB NF dependence on LO power, RF or IF frequency, or on a range of parameter values. Schematic files Mix_XX_SSBNF_LOswp, Mix_XX_SSBNF_FRFswp, and Mix_XX_SSBNF_PRMSwp and the corresponding display files with the same name are available for this purpose.

Example: Effect of device width on noise figure in a Gilbert cell mixer

The RF signal input is generally applied to the lower tier differential input in the MOS Gilbert mixer. The width of these devices will influence the noise properties of the mixer [5], so it is good to evaluate this effect by sweeping the device width and observing noise figure dependence. [Differential amplifier as lower tier of an XOR \(Gilbert\) multiplier.](#) shows the schematic of this input amplifier.



Differential amplifier as lower tier of an XOR (Gilbert) multiplier.

The range of parameters to be swept is entered into the schematic Mix_Diff_SSBNF_PRMSwp as shown in [Defining the parameter to be swept in the schematic and the parameter sweep range.](#)



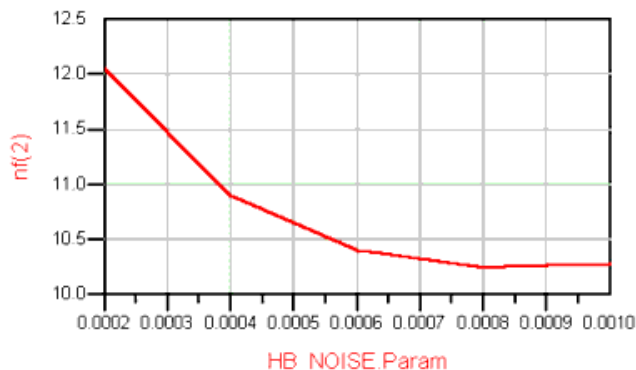
```

ParamSweep
Sweep1
SweepVar="Param"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=2e-4           Set the parameter
Stop=1e-3            sweep range and
Step=2e-4            step size

```

Defining the parameter to be swept in the schematic and the parameter sweep range.

As width W1 is swept, we see a minimum in noise figure at a width of about 800 nm in [Plot of output from Mix_Diff_SSBNF_PRMSwp.dds display file.](#) This is in approximate agreement with the noise model described in Reference [5]. In the figure, MOSFET width W1 is the swept parameter (Param). W1 is in units of meters.



Plot of output from Mix_Diff_SSBNF_PRMSwp.dds display file.

Note

This simulated noise figure may not agree exactly with the one that you measure with a hot-cold source noise figure meter by placing a bandpass filter in front of the mixer. This is because the out-of-band mismatch of the filter (S_{11} and $S_{22} = 1$ outside the passband) will reflect any LO or IF components appearing at the mixer input back into the mixer. The remixing that occurs will affect the noise figure in some types of mixers.

The second type of mixer noise figure measurement supported by the DesignGuide schematics is based on the Hot-Cold method referred to above. The schematics (Mix_XX_HotColdNF, Mix_XX_HC_NF_LO_RFswp, and Mix_XX_HotColdNF_PRMSwp) are configured without any input filters, so a noise figure simulation based on signals at both RF and Image frequencies, and noise at all other LO harmonic images is performed. This is sometimes referred to as the Double-Sideband Noise Figure, but might be more appropriately called the *All-Sideband* noise figure. The noise figure simulated by this method should agree with that measured with a noise figure measurement instrument (assuming the device models for noise are accurate) because it employs the same technique.

A Single Sideband NF can also be obtained by placing a bandpass filter (from the Filters-Bandpass component palette) between the noise source and the mixer RF input. This is similar to the approach that would be used experimentally. However, that this SSB measurement does not provide the NF specified by the IEEE standard [3,4]. Also, the out-of-band reflections will affect the measurement and simulation as described in the preceding note above.

Analysis	Schematic ()	Display
Single sideband noise figure	Mix_SE_SSBNF	Mix_SE_SSBNF
Single sideband noise figure with LO power sweep	Mix_SE_SSBNF_LOswp	Mix_SE_SSBNF_LOswp
Single sideband noise figure with parameter sweep	Mix_SE_SSBNF_PRMSwp	Mix_SE_SSBNF_PRMSwp
Single sideband noise figure with RF input frequency sweep	Mix_SE_SSBNF_FRFswp	Mix_SE_SSBNF_FRFswp
All sideband noise figure	Mix_SE_HotColdNF	Mix_SE_HotColdNF
All sideband noise figure with LO power and input frequency sweeps	Mix_SE_HC_NF_LO_RFswp	Mix_SE_HC_NF_LO_RFswp
All sideband noise figure with parameter sweep	Mix_SE_HotColdNF_PRMSwp	Mix_SE_HotColdNF_PRMSwp

Design and display files for noise figure simulations.

Large Signal Mixer Simulations

Many applications require the mixer to be free of distortion for rather large input signal levels. Distortion leads to the generation of harmful odd-order intermodulation products (intermodulation distortion or IMD) that can produce spurious signals that may interfere

with the desired signal at the IF frequency. Second-order distortion is also of concern for direct-conversion receiver designs. Harmonic distortion (HD) also can occur but is usually not a serious interferer as subsequent IF filtering can generally remove it.

This DesignGuide provides two techniques for assessing the large signal performance: gain compression and two-tone IMD simulations. Of the two, the two-tone simulation should provide the most accurate information and gives both second-order-intercept and third-order-intercept as figures of merit. (See the Fundamentals of Mixer Design DesignSeminar CD [1] for definitions.)

Gain Compression

Two types of gain compression simulation schematics and displays are provided. First, the Mix_XX_GC schematic simulates the conversion gain of a mixer as a function of RF input power. You can set the range of RF input powers. The corresponding display files Mix_XX_GC present IF spectra and plots of conversion gain vs. RF input power and IF output power, for both down and up conversion. This simulation allows you to see the details of the gain compression; that is, whether it compresses quickly or slowly as you increase the RF power level at the input.

If you are just interested in finding the input power required for a particular level of gain compression, then the Mix_XX_PNdB, Mix_XX_PNdB_LOswp, and Mix_XX_PNdB_PRMswp schematic files are used to determine this input power for N dB of gain compression. The standard LO and user-defined parameter sweeps are available as usual. Gain compression as a function of input RF frequency can also be simulated for the cases where the LO tracks the RF frequency to give a constant IF output frequency, or for fixed LO and variable IF frequency (Mix_XX_PNdB_FRFswp). These simulations have previously been described.

Two-Tone Intermodulation Distortion

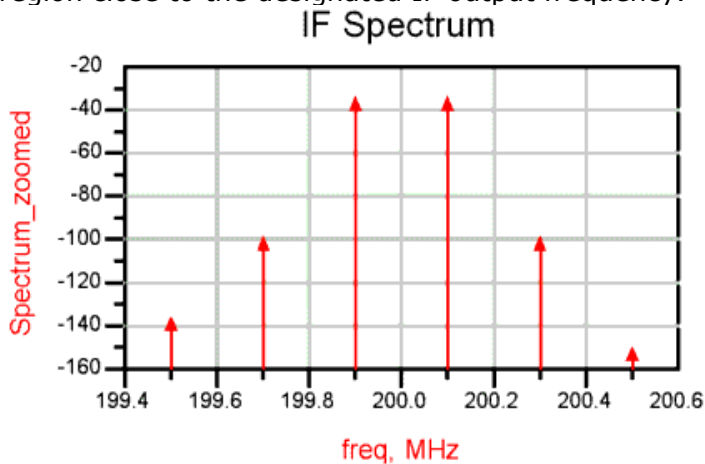
A more sensitive way to evaluate the large signal handling capability of a mixer is to apply two or more signals to the input. These dual or multiple signals (tones) mix together and form intermodulation products. Two tone simulations are used in the Mixer DesignGuide to evaluate the intermodulation distortion (IMD) generation of your mixer. The results are expressed in terms of the carrier-to-IMD power ratio (dB) and calculated second- (SOI) and third-order (TOI) intercepts. These results are representative of how well the mixer will perform in a true multicarrier environment. In some cases, you will want to evaluate the mixer's intercept or IMD power as a function of such variables as LO power, DC bias, device widths, resistances or load impedances, and possibly many others.

All of the following simulation files require that you select the RF center frequency (RFfreq), LO frequency (LOfreq), and a spacing frequency, Fspacing, between the two input signals. Thus, the two RF inputs are located at RFfreq +/- Fspacing/2. You must also specify the load impedance, Zload, and in some cases, source impedance, Zsource.

VAR	
Eq1	R1
LOfreq=1601 MHz	Set the following parameters:
RFfreq=200 MHz	1) LO frequency, LOfreq.
Fspacing=200 KHz	2) Center frequency of the two input tones, RFfreq.
Zload=400+j*0	3) Frequency spacing between tones, Fspacing.
Zsource=100+j*0	4) Load and source impedance, Zload, Zsource
P_LO=3	5) LO power, P_LO

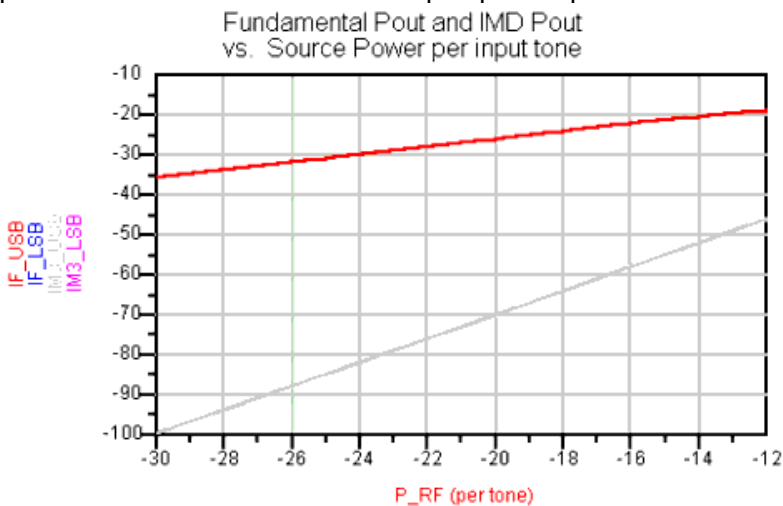
Setup for mixer TOI simulation

The first simulation template, Mix_XX_TOI, is used to provide a spectral display and to calculate IMD ratio, SOI, and TOI at a fixed RF input power and LO input power. Thus, P_LO and P_RF must be specified. If your LO source is non-sinusoidal, you may wish to the harmonic amplitudes on the P_nHarm source to higher levels than 100 dB below the fundamental. Harmonics higher than the third may be added, also. You must also specify the Maximum IMD order that you are interested in displaying on the spectral plot. Do not use IMD orders that are much higher than necessary, as it will increase the computation time and data file size. A single display file shows the results for both up and down conversion. Close-ups of the IF output spectrum at both the up- and down-conversion frequencies are shown automatically as in [Zoomed spectral display of IMD power output from the mixer for fixed RF and LO power levels.](#) The display zooms automatically to the region close to the designated IF output frequency.



[Zoomed spectral display of IMD power output from the mixer for fixed RF and LO power levels.](#)

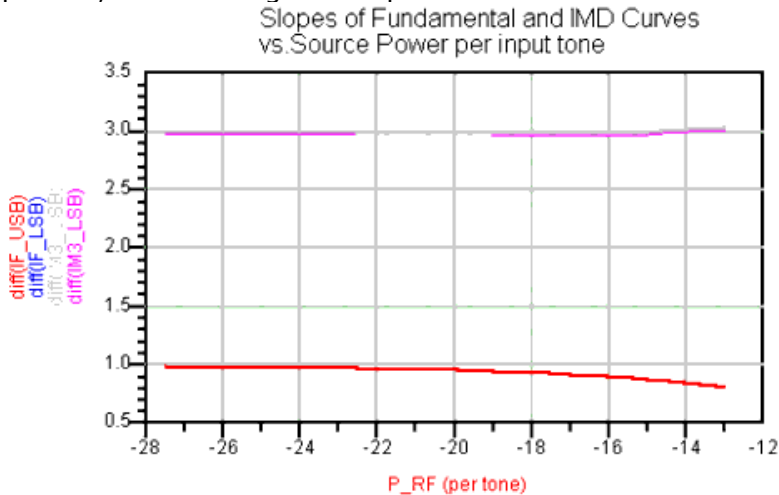
This simulation will provide essentially one data point - projected performance from a single RF input power level. To determine how ideally the mixer is performing, and thus find out if the intercept calculations are valid, you must sweep the RF power and determine if the slope of the third order IMD power is close to 3. Use Mix_XX_TOI_RFswp for this purpose. [Fundamental and IMD output powers from the mixer as a function of RF input power.](#) shows a plot of the fundamental IF output, Pout, and the third-order IMD power as a function of the RF input power per tone.



[Fundamental and IMD output powers from the mixer as a function of RF input power.](#)

Another plot (shown in [Slope of the fundamental and IMD power outputs from the mixer](#)

as a function of RF input power per tone.) is provided that presents the IF fundamental and IMD slopes vs. P_RF. If the slope is substantially off, you may need to increase the LO order on the harmonic balance controller to improve accuracy. Occasionally, increasing oversampling is also beneficial. The TOI calculation can be performed at any of the swept RF power levels by using the slide marker to set the power level. The calculated TOI will only be valid when the slope is equal to 3. At high signal levels, some of the higher order (5th, 7th, ...) IMD products also fall on third-order frequencies. This often results in a slope other than 3. Thus, intercepts are best calculated from data taken at lower input powers, well below gain compression.



Slope of the fundamental and IMD power outputs from the mixer as a function of RF input power per tone.

Other two-tone simulation sweeps : (Schematics: Mix_XX_TOI_LOswp, Mix_XX_TOI_PRMswp, and Mix_XX_TOI_FRFswp; Display files that correspond to these schematics have the same names)

TOI simulation files are also provided to sweep the RF input center frequency, RFreq, the LO power, P_LO, or an arbitrary parameter, Param. In all cases, the range of the swept quantities must be defined as part of a sweep plan as shown in [Sweep Plan is used to specify the swept parameter range.](#) The LO sweep and Parameter sweeps are useful for optimizing the mixer IMD performance which may vary with LO power, bias currents, device widths, and load resistances and impedances. The FRF sweep steps the RF input frequency and allows you to plot mixer IMD performance over an input frequency band. Note that all of these sweeps are at a fixed RF input power, so it is important to determine first that the mixer behaves normally (third-order IMD slope = 3) before using TOI as an optimization criteria. This procedure is described above.

```
SweepVar="P_LO"
SweepPlan="Coarse"
```

SWEEP PLAN

```
SweepPlan
Coarse
Start=-5 Stop=-5 Step=5.0 Lin=
UseSweepPlan=
SweepPlan=
Reverse=no
```

Sweep Plan is used to specify the swept parameter range.

[Design and display files for large-signal two-tone simulation](#) shows Design files for large-

signal two-tone simulations.

Design and display files for large-signal two-tone simulation

Analysis	Schematic ()	Display
Intermodulation distortion - Second and Third-order intercept calculation - IMD spectrum	Mix_SE_TOI	Mix_SE_TOI
Intermodulation distortion - Third-order intercept calculation - swept LO power	Mix_SE_TOI_LOswp	Mix_SE_TOI_LOswp
Intermodulation distortion - Third-order intercept calculation - swept RF input power	Mix_SE_TOI_RFswp	Mix_SE_TOI_RFswp
Intermodulation distortion - Third-order intercept calculation - swept RF frequency.	Mix_SE_TOI_FRFswp	Mix_SE_TOI_RFswp
Intermodulation distortion - Third-order intercept calculation - swept parameter	Mix_SE_TOI_PRMswp	Mix_SE_TOI_FRFswp

Spurious Free Dynamic Range

A separate display has been provided for evaluation of the Spurious Free Dynamic Range (SFDR). This represents the difference between the minimum detectable input signal power (MDS) and the input power required to produce a third-order IMD power just equal to the MDS. Because MDS depends on noise figure, the results of both noise figure and TOI are required. Since SFDR is a function of input power, the TOI simulation must include the RF power sweep. Thus, Mix_XX_TOI_RFswp is the appropriate simulation panel. The Dynamic_range display panel requires selection of the TOI output as its dataset. The noise figure input, generally simulated with a single-sideband NF analysis, is assumed to be independent of RF input power. Thus, a single NF is provided as a parameter, entered as an equation. MDS also depends on bandwidth. This must be entered manually as follows.

Eqn NF=8.0 Enter noise figure simulation data

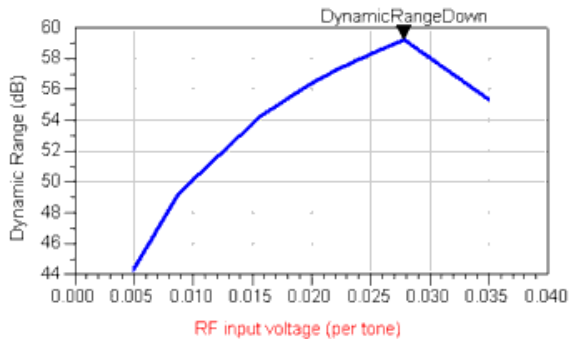
Eqn BW=3e7 Enter signal bandwidth

Noise figure and bandwidth must be entered into the Dynamic Range display.

The SFDR is then plotted as a function of two-tone RF source available power and RF input voltage. Separate plots are provided for the upconversion and downconversion applications. [Spurious-free dynamic range as function of RF input voltage.](#) illustrates one of these plots.

Downconversion Mixer

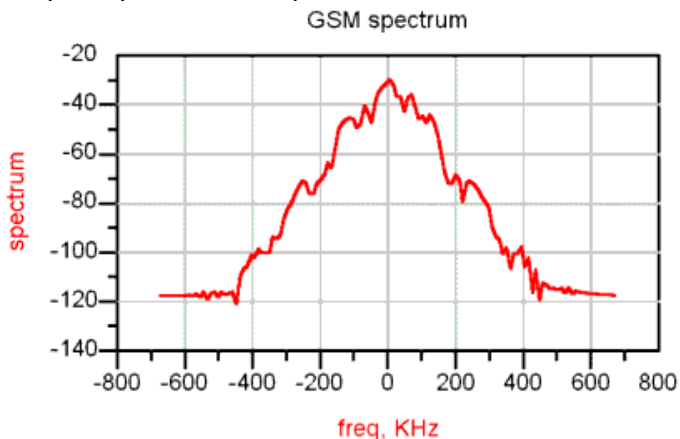
RF Input Voltage (V)	Dynamic Range (dB)	Available Source Power
0.028	59.245	-31.000



Spurious-free dynamic range as function of RF input voltage.

Digital Modulation Tests

While the two-tone evaluation provides guidance on design tradeoffs that will improve mixer IMD performance, it is not sufficient to guarantee that adjacent channel power (ACP) specification will be met when digital modulation or multicarrier signals are present at the mixer input. Thus, Circuit Envelope simulations using digital modulation sources can be used to simulate the output spectrum and measure ACP. Two sources have been provided for illustrations of the technique. Simulations of GSM and CDMA data sources are given in the schematic and display files GSMtest and CDMAtest. An example of the output spectra simulated with the GSM test is shown in [Simulated mixer IF output spectrum for a GSM digital signal input.](#) Note that the circuit envelope simulations can generate very large data files, you should refer to the ADS documentation on this type of simulation. The frequency axis of the plot is centered around the IF output frequency.



Simulated mixer IF output spectrum for a GSM digital signal input.

[Circuit envelope simulations for digital modulation](#) shows Circuit envelope simulations for digital modulation.

[Circuit envelope simulations for digital modulation](#)

Analysis	Schematic ()	Display
GSM data source	GSMtest	GSMtest
CDMA data source	CDMAtest	CDMAtest

Other Frequency Conversion Devices

The additional capabilities for frequency conversion applications include:

- Static frequency dividers (both MOS and BJT MSFFs)
 - Injection locked frequency divider (MOS)
 - Active and passive frequency doubler designs
- While there are many possible implementations of these circuits, a few representative subnetworks are provided as a starting point for design or to become familiar with the use of these simulation templates. Many of these simulations require use of the Transient Assisted Harmonic Balance method to achieve convergence, so they can also be used as example files for TAHB simulations.

Static Frequency Dividers

The most commonly used static frequency divider employs a master-slave flip-flop with the output inverted and connected back to the input. This T-connected FF then divides by 2. Of course, other variations can be made for larger divide moduli using additional FFs cascaded in shift register fashion (synchronous dividers) often with extra control logic to select between two or more moduli. At present, the simulation files are provided for the simple divide-by-2 T-FF.

These examples are typical emitter or source-coupled differential latches. The DC bias and amplitude of the clock input is external and must be set by the user. The Source Coupled Inverter is provided as a load device to give representative fanout in the MOS divider simulations. The following table describes the simulation types provided.

Static frequency divider simulation files

Design File Name	Description
DivBy2_TAHB	BJT divider. TAHB simulation. Sinusoidal clock frequency sweep.
DivBy2_Pulse_TAHB	BJT divider. TAHB simulation. Pulse clock frequency sweep.
DivBy2_Transwp	BJT divider. Transient simulation. Pulse clock frequency sweep.
DivBy2_MOS_TAHB	MOS divider. TAHB simulation. Sinusoidal clock frequency sweep.
DivBy2_MOS_Pulse_TAHB	BJT divider. TAHB simulation. Pulse clock frequency sweep.
DivBy2_MOS_Transwp	BJT divider. Transient simulation. Pulse clock frequency sweep.
PulseSourceTest	Evaluate and set up differential pulse clock source.
DivBy3_wPhSwitchedDFFs	Behavioral divider. Transient simulation. Pulse clock source.
DivBy3_Trans	MOS divider. Transient simulation. Pulse clock source.
DivBy3_TAHB	MOS divider. TAHB simulation. Sinusoidal clock frequency sweep.
DivBy5_wPhSwitchedDFFs	Behavioral divider. Transient simulation. Pulse clock source.

Simulations that include TAHB generally provide both transient and harmonic balance display pages accessible through the page menu on the data display. Sweeps are provided so that the maximum clock frequency can be quickly determined. Phase noise generation by the divider is also displayed. If driving clock sources with phase noise are substituted, the phase noise reduction provided by the divider can also be seen. Ideally, a divide-by-2 function should reduce input phase noise by 6 dB.

Injection Locked Frequency Dividers

Injection locking of oscillators is an old concept[12], generally used to improve phase noise and stability. Oscillators can also be injection locked by a higher input frequency at twice the natural frequency of oscillation. In this way, they can be used in a divide-by-2 function, though over a much narrower frequency range than the static dividers above[13]. The benefit, though, is much lower power dissipation than the equivalent function in a static or dynamic divider, and operating frequencies that can more closely approach the f_{max} of the transistor, rather than typically 20 - 40% of f_T in the case of static dividers. The Injection-Locked Frequency Divider (ILFD) set of simulations is sequenced from analysis of the basic MOS differential free running oscillator, parameter sweeps, phase noise simulation, through a lock range simulation of the same oscillator when injection locked.

Begin with the free running oscillator simulation to determine the oscillation frequency. It is necessary to set this correctly at the desired output frequency because the ILFD often has rather narrow operating frequency range. Then proceed to the divider simulations. Table 2-10 lists the design files available for simulation. Simulation of frequency division generally requires transient-assisted harmonic balance to obtain convergence.

Simulation design files for injection locked frequency divider simulation

Design File Name	Description
ILFD_free_run	HB free running oscillator simulation for the differential MOS oscillator (DILFD_core)
ILFD_free_run_PRMswp	HB parameter sweep of the free running oscillator. This can be used to vary current, or other design parameters.
TAHB_ILFD_free_run	Occasionally, the HB simulation fails to find convergence. The transient-assisted HB provides a set of initial conditions that enables HB to quickly find the steady state solution.
TAHB_ILFD_free_run_PRMswp	TAHB version of the free running oscillator parameter sweep.
TAHB_ILFD_locked	TAHB simulation of the locked oscillator.
TAHB_ILFD_lockrange	Simulation of the locked oscillator with frequency sweep. Note that the simulation will occasionally stop before completing the entire sweep when the oscillator loses lock. But, it will stop after losing lock, so the lock range is still found.
DILFD_core	Basic MOS differential oscillator subnetwork

Frequency Doubler Simulations

Occasionally there are applications where it may be preferable to double the frequency of an oscillator instead of designing one with fundamental output at the desired frequency[14][15][16]. Many instruments such as sweepers and synthesized generators have used frequency doublers to extend the range available for their use. This type of application requires a wide frequency range of operation. An example of a passive diode full-wave frequency doubler is provided in the example subnetworks that has a multi-octave range. Simulation examples are also provided for optimization of the matching networks for wideband application.

Two active frequency doubler example subnetworks are also given. Due to the bandwidth limitations of the MOS devices used in these examples, they are tuned rather than wide band. These include a mixer (double balanced Gilbert mixer) with both inputs connected to the same source and a MOS tuned amplifier with output tuned to twice the input frequency.

List of design simulation files and subnetworks provided in the frequency doubler simulations

Design file name	Description
FreqDoublers	Wideband diode full-wave frequency doubler subnetwork
Diff_MixerUnderTest_Tuned_D2SE	Tuned Gilbert mixer subnetwork from existing mixer menu. this is also used in the upconversion examples of the mixer design guide.
Doubler_MOS_TA	MOS tuned amplifier frequency doubler subnetwork.
FreqDoublers_FWdiode	Simulation of wideband frequency doubler with source voltage sweep.
FreqDoublers_Gilbert	Simulation of tuned Gilbert mixer frequency doubler (0.9 to 1.8 GHz) Source voltage sweep.
FreqDoublers_MOS_TA	Simulation of MOS tuned amp frequency doubler (1.0 to 2.0 GHz). Source voltage sweep.
MOS_TADoubler_Opt	Optimize FET width and output for narrowband doubler
InputMatchOpt	Optimize the input match of the full-wave diode wideband doubler.
OutputMatchOpt	Optimize the input and output match for the full-wave wideband doubler.

References

Note

The EESof Application website contains additional reference material for mixer design and frequency converters and modulators
http://www.home.agilent.com/agilent/redirector.jsp?action=ref&cname=AGILENT_COLLECTION&key=1411747&cc=US&lc=eng

1. S. Long, Fundamentals of Mixer Design, Agilent EESof Design Seminar, 1999. [NOTE: available from the EESof Application web site
<http://cp.literature.agilent.com/litweb/pdf/5989-9102EN.pdf>]
2. S. Long, RFIC MOS Gilbert Cell Mixer Design, Agilent EESof Design Seminar, 1999. [NOTE: available from the EESof Application web site
<http://cp.literature.agilent.com/litweb/pdf/5989-9103EN.pdf>]
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4. IRE Subcommittee 7.9 on Noise, "Description of the Noise Performance of Amplifiers and Receiving Systems", Proc. IEEE, vol. 51, pp 436-442, 1963.
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14. P. Kangaslahti et al., "Low Phase Noise Signal Generation Circuits for 60 GHz Wireless Broadband Systems," IEEE Int. Microwave Symp., Paper TU2-B3, pp. 40-43, June 2000.
15. K. Kimura and H. Asazawa, "Frequency Mixer with Frequency Doubler for Integrated Circuits," IEEE J. Solid State Cir., Vol. 29, No. 9. pp.1133-1137, Sep. 1994.
16. F. Ellinger and H. Jackel, "Ultracompact SOI CMOS Frequency Doubler for Low Power Applications at 26.5-28.5 GHz," IEEE Microwave and Wireless Components Lett., Vol. 14, No.2, pp. 53-55, Feb. 2004.

Mixer QuickStart Guide

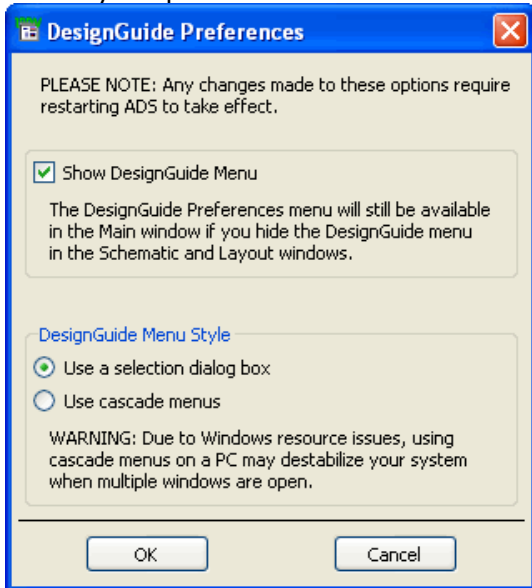
The Mixer DesignGuide is integrated into the Agilent EEs of Advanced Design System. It contains many analysis schematics and data displays for the design and analysis of RFIC mixers, frequency multipliers and dividers, and the application of discrete mixers in RF systems.

Display Preferences

DesignGuides can be accessed in the Schematic window through either cascading menus or dialog boxes. You can configure your preferred method in the Main, Schematic, or Layout window. Choosing **Preferences** brings up a dialog box that enables you to:

Note
Use the dialog box menu style on Windows systems because resource issues typically make the operating system unstable.

- Disable all DesignGuide menu commands except Preferences in the Main window and remove the DesignGuide menu in the Schematic and Layout windows.
- Select your preferred interface method (cascading menus vs. dialog boxes).



Close and restart the program for your preference changes to take effect.

Accessing Documentation

To access the documentation for the DesignGuide, select either of the following:

- **DesignGuide > Mixer > Mixer DesignGuide Documentation** (from ADS Schematic window)
- **Help > Topics and Index > DesignGuides > Mixer** (from any ADS window)

Mixer DesignGuide Features

- Passive and active mixer library
- Single-ended and differential Input/Output simulation schematics
- Up or Down conversion

- Sweeps of local oscillator and RF power, LO and RF frequencies, and user-defined parameters
- Analysis templates for:
 - DC Biasing
 - Output spectrum, conversion gain, port impedances, and isolation simulations
 - Gain compression
 - Intermodulation distortion and intercepts
 - Noise figure
 - Dynamic Range
 - Adjacent channel power with digital modulation
- Frequency multipliers and dividers:
 - Static frequency dividers
 - Injection locked frequency dividers
 - Passive and active frequency doublers
- Impedance matching networks

Note
The DesignGuide is not a complete solution for mixer and RF system designers, but will provide you with some useful tools. It is intended to save you time in setting up schematics and displays.

Mixer DesignGuide Contents

The Mixer DesignGuide is made up of simulation files and utilities to facilitate your design and analysis of mixers. From an ADS Schematic or Layout window, choose **DesignGuide** > **Mixer DesignGuide** to display the schematics and tools organized in the following categories. <div align="left">

Category	Description
Device Characterization	Curve-tracer schematics for BJTs, NMOS, and PMOS. The schematics for DC bias point evaluation of active mixer circuits can be used to determine the proper DC bias conditions and device widths to be used in a mixer. Also includes two sample MOSFET BSIM3 device model parameter sets.
Example Mixers	Library of mixer examples that can be used as a starting point for your own design.
Differential and Single-Ended Mixer Characterization	Characterizations for Differential and Single-Ended mixers can be selected with no swept parameters, with swept LO power, swept input frequency, or a user-defined arbitrary swept parameter. These options are useful for finding the optimum LO power, bandwidth, and parameters such as device widths or component values respectively.
Mixer Examples with Modulated Signals	Schematics for simulation of mixers driven by digital modulation types such as GSM or CDMA.
Matching Networks	Lumped 2 element and multi-element matching network schematic templates to design a matching network to interface between stages or to the off-chip (usually 50 ohm) environment using known input and output impedances or admittances. The S-parameters determined by the schematic called <i>Mixer Characterization > IF Spect, Isolation, Conv. Gain, Port Impedances</i> can be used in conjunction with these network design tools to match to a known source or load impedance.
Transistor Bias Utility	The Transistor Bias Utility provides SmartComponents and automated-assistants for the design and simulation of common resistive and active transistor bias networks. The automated capabilities can determine the transistor DC parameters, design an appropriate network to achieve a given bias point, and simulate and display the achieved performance. All SmartComponents can be modified when selected. You simply select a SmartComponent and with little effort redesign or verify their performance.
Smith Chart Utility	The Smith Chart Utility provides full smith chart capabilities, synthesis of matching networks, allowing impedance matching and plotting of constant Gain/Q/VSWR/Noise circles.
Impedance Matching Utility	The Impedance Matching Utility performs the synthesis of lumped and distributed impedance matching networks based on provided specifications. The Utility features automatic simulation, sensitivity analysis, and display setup to enable simple and efficient component verification.
Frequency Multipliers and Dividers	From an ADS Schematic or Layout window, choose DesignGuide > Freq Multipliers and Dividers to view the example subnetworks, design simulation, and displays for the following types of frequency translation devices. Static frequency dividers Injection locked frequency dividers Frequency doublers

Using Mixer Characterizations

The characterization items have identical options, which can be used to select the type of analysis. When this final selection is made, a schematic with a sample mixer will be copied into your workspace. Previously simulated results, using the sample mixer, are displayed by the associated data display file that is opened automatically.

To use this as a template for your own designs, substitute your own mixer schematic in the mixer subnetwork. Push into the subnetwork, delete the existing mixer (but keep the ports), and replace it with your own design. Return to the top-level schematic, set the simulation parameters, and run a simulation. If you keep the top-level schematic name, the corresponding data display will be updated automatically. Also, note that you must provide your own verified nonlinear device models to get accurate simulation results.

- Simulation control parameters that need to be set are enclosed in red boxes on the schematics, as follows.

VAR
R2

LOfreq=855 MHz
 RFFreq=900 MHz
 P_RF=-30
 P_LO=0
 Zload=400+j*0

Set the following parameters:

- 1) LO frequency, LOfreq
- 2) Input frequency, RFFreq
- 3) Input power, P_RF
- 4) LO power, P_LO
- 5) Load impedance, Zload

- Data displays that use many equations have the equations on a separate page. See the Page menu.
- Some data displays have more than one page of output. Again, see the Page menu.
- In all mixer characterization schematics, *RFFreq* is the variable defining the input signal frequency and *IFfreq* is the variable defining the output frequency. If *RFFreq* is higher than *IFfreq*, the simulation is set up for down-conversion. If you want to simulate up-conversion, define *RFFreq* and *IFfreq* such that $IFfreq > RFFreq$.